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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,281	09/07/2004	Chi Chang	12234-US-PA	5280

31561 7590 09/19/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

KARIMY, MOHAMMAD TIMOR

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

24

Office Action Summary	Application No.	Applicant(s)	
	10/711,281	CHANG, CHI	
	Examiner	Art Unit	
	Mohammad Timor Karimy	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters; prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claim 1 recites the limitations “close to the device area” in line 10 and “overstride” in line 11. In the interest of clarity, examiner suggests that applicant change “close to the device area” to “**closest** to the device area” and “overstride” to “**overlap**”.

Claim 2 recites the limitations “close to the device area” in line 2. Examiner suggests that applicant change “close to the device area” to “**closest** to the device area” to better address the limitation.

Claim 6 recites “which” in line 2 that appears to a grammatical error. Examiner suggests applicant changes “which” to “**where**”.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 recites the limitation “**the** farthest bonding pads” in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites the limitation “**the** part of the Nth layer” in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US 6,759,329 B2).

Cheng discloses in figures 5a-5b and in columns 5-6, a circuit layout structure for a chip with a bonding pad area (see figure 5b below), an adjacent device area (see figure 5b below), and a substrate comprising:

a plurality of circuit layers (M1-M5), sequentially stacking over the substrate (although substrate is not shown in figures 5a-b, Cheng explicitly mentions the conductor layers being on a substrate in column 5 line 32);

a plurality of dielectric layers (Cheng mentions insulating layers between conductive layers in column 5 line 33), each sandwiching between a pair of neighboring circuit layers, and

a plurality of vias (Cheng mentions vias connecting various conductive layers in column 5 lines 52-53), passing through the dielectric layers and electrically connecting various circuit layers (M1-M5),

wherein the circuit layer farthest M5 from the substrate has a plurality of bonding pads (22, 24 and M6 in figure 5b) within the bonding pad area (show in fig.), and the

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bonding pads close to the device area (24 and M6) **overstride** at least a non-signal circuit layer M2 (signal bus 26 overlaps non-signal bus power and ground bus) within the device area via the circuit layer farthest from the substrate (M5), and then electrically connects with the circuit layer closer to the substrate M1 through the via.

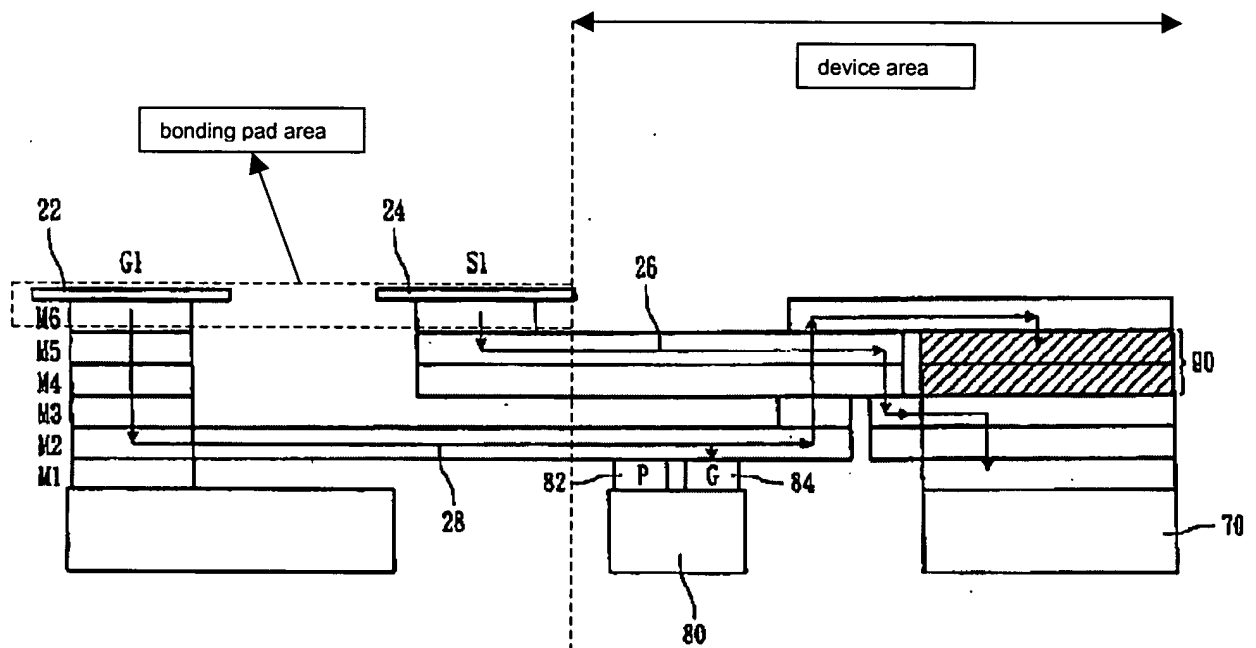


FIG. 5b

With respect to claim 2, Cheng discloses the circuit layout structure of claim 1, wherein the bonding pads **close** to the device area (24 and M6 in figure 5b or the plurality of inner row pads in shown in figure 5a) comprises a plurality of signal bonding pads.

With respect to claim 3, Cheng discloses the circuit layout structure of claim 1, wherein the bonding pad 22 farther away from the device area comprises a plurality of non-signal bonding pads (power or ground).

With respect to claim 4, Cheng discloses the circuit layout structure of claim 3, wherein the bonding pads 22 farther from the device area comprises a ground bonding pad.

With respect to claim 5, Cheng discloses in figures 5a-b, column 5 lines 20-23 and column 6 lines 10-13 the circuit layout structure of claim 3, wherein the bonding pads next to the farthest bonding pads from the device area comprises a power bonding pad (note that Cheng does not explicitly teach that bonding pad 21 being the farthest from the device area is the ground; however, Cheng teaches the power and ground arrangement in figures 5a-b, and Cheng explicitly teaches in column 6 lines 10-13 that bonding pad 22 which is ground in figure 5b can be used as the power bonding pad – one of the ordinary skill in the art would recognize such an arrangement making the farthest bonding pad 22 as the ground and the bonding pad next to the farthest pad as the power bonding pad).

With respect to claim 6, Cheng discloses the circuit layout structure of claim 1, wherein the circuit layers comprises N circuit layers **which** N is a natural integer greater than 2, and the first circuit layer of N circuit layers is set on the substrate, a (N-1)th circuit layer is set on a (N-2)th circuit layer, and a Nth circuit layer is set on the (N-1)th

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circuit layer and the part of the Nth circuit layer within the device area forms a direct electrical connection with the bonding pad closest to the device area (the Nth circuit layer is M5 in figure 5b).

With respect to claim 7, Cheng discloses the circuit layout structure of claim 6, wherein the bonding pad farthest from the device area comprises a ground bonding pad such that the ground bonding pad forms a direct electrical connection with the (N-2)th (M3) circuit layer (note that Cheng does not explicitly teach that bonding pad 21 being the farthest from the device area is the ground; however, Cheng teaches the power and ground arrangement in figures 5a-b, and Cheng explicitly teaches in column 6 lines 10-13 that bonding pad 22 which is ground in figure 5b can be used as the power bonding pad – one of the ordinary skill in the art would recognize such an arrangement making the farthest bonding pad 22 as the ground and the bonding pad next to the farthest pad as the power bonding pad).

With respect to claim 8, Cheng discloses the circuit layout structure of claim 6, wherein the bonding pad next to the farthest bonding pad from the device area comprises a power bonding pad such that the power bonding pad forms a direct electrical connection with the (N-1)th (M4) circuit layer (note that Cheng does not explicitly teach that bonding pad 21 being the farthest from the device area is the ground; however, Cheng teaches the power and ground arrangement in figures 5a-b, and Cheng explicitly teaches in column 6 lines 10-13 that bonding pad 22 which is ground in figure 5b can be used as the power bonding pad – one of the ordinary skill in

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the art would recognize such an arrangement making the farthest bonding pad 22 as the ground and the bonding pad next to the farthest pad as the power bonding pad).

With respect to claim 9, Cheng discloses the circuit layout structure of claim 6, wherein the bonding pad next to the closest bonding pad from the device area (note 22 in figure 5b) is electrically connected through the (N-1)th circuit layer to the Nth circuit layer within the device area (see fig. 5b above).

Conclusion

8. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure. Shinogi et al. (US Pub. 2003/0011073 A1), Nojiri (US Patent 6,489,689 B2) and Crowder et al. (US Patent 5,446,243) discuss the use of power and ground lines, signal lines, multilevel metallization layers with dielectric layers in between and vias.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-2006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mtk



N. DREW RICHARDS
PRIMARY EXAMINER